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**APPLICATION FOR UNITED STATES PATENT**

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**Title:** MEMS PACKAGE

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**SPECIFICATION**

## **A WAFER-LEVEL THROUGH-WAFER PACKAGING PROCESS FOR MEMS AND MEMS PACKAGE PRODUCED THEREBY**

### **Field of the Invention**

The present invention relates to a wafer-level packaging process for MEMS applications, and more specifically, to a method for putting electrical feed-throughs through an SOI wafer.

### **5     Background of the Invention**

In microelectromechanical systems (MEMS), the functional element, such as a circuit, sensor or actuator, must often be separated from the environment, yet electrical signals must be sent to and received from the functional element. The functional elements are flexible structures operable within a hermetically sealed cavity.

10   The challenge in packaging MEMS is achieving the electrical connection without opening the cavity to the environment, and to do this with a simple process that results in a small overall footprint and outline. In other words, the MEMS should be fabricated to form a functional element within a hermetically sealed cavity in the semiconductor wafer having an overall structure of small dimension both laterally and vertically.

Past and current attempts to achieve such MEMS include die-level hermetic packaging, but this method produces a device with a large package size at a high cost. Another example is a buried feed-through, but this is a relatively complex process. Still another example is first bonding, then sealing open areas with high  
5 temperature LPCVD films, but high temperature processing is not compatible with many metals present on the wafers.

A need thus exists in the semiconductor industry for a method for wafer-level packaging for MEMS applications that allow small footprints, small chip outlines, low-temperature processing, hermetic sealing, and low cost.

## 10 **Summary of the Invention**

The present invention provides a wafer-level packaging process for MEMS applications in which a SOI (silicon-on-insulator) wafer is bonded to a MEMS wafer and the electrical feed-throughs are achieved through the SOI wafer. The process of the present invention is a simple procedure involving no high temperatures and  
15 results in a small, thin device with functional elements hermetically sealed therein. To this end, the method includes providing a first substrate having the functional element thereon connected to at least one metal lead, and providing a second SOI substrate having a recessed cavity in a silicon portion thereof with metal connectors formed in the recessed cavity. The non-recessed surfaces of the second SOI substrate are bonded to  
20 the first substrate to form a hermetically sealed cavity. Within the cavity, the metal leads are bonded to respective metal connectors. Prior to bonding, the recessed cavity has a depth that is greater than the thickness of the functional element and less than the combined thickness of the metal leads and their respective metal connectors. After bonding, silicon from the second SOI substrate is removed to expose the buried oxide  
25 portion of the second SOI substrate. Metal pads are then formed through the second

SOI substrate to the metal connectors within the cavity, such as by etching vias in the substrate and depositing the metal pads within the vias. Wire bond pads are thereby connected to the functional element without opening the cavity to the environment. Electrical signals may then be fed through the SOI wafer to the metal connectors, metal leads and the functional element. In one embodiment of the method of the present invention, an oxide layer is grown on the SOI wafer both on the surface to be bonded to the first substrate and within the recessed cavity to provide electrical isolation between electrical connectors. In yet another embodiment of the method of the present invention, a passivation layer is applied over the buried oxide layer of the SOI substrate and over the metal pads.

#### **Brief Description of the Drawings**

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with a general description of the invention given above, and the detailed description given below, serve to explain the invention.

FIGS. 1-9 schematically depict an embodiment of the method of the present invention for packaging a MEMS device, wherein:

FIG. 1 depicts the starting first substrate;

FIG. 2 depicts formation of a functional element and metal leads on the first substrate;

FIG. 3 depicts the starting second SOI substrate;

FIG. 4 depicts the formation of a recessed cavity in a silicon portion of the second SOI substrate;

FIG. 5 depicts the formation of the metal connectors within the recessed cavity;

FIG. 6 depicts the bonding of the first substrate to the second SOI substrate and the bonding of the metal connectors to the metal leads;

5           FIG. 7 depicts the removal of the second silicon portion of the SOI substrate to expose the buried oxide layer;

FIG. 8 depicts the formation of vias through the SOI wafer to expose the metal connectors within the recessed cavity; and

FIG. 9 depicts the formation of the metal pads within the vias for  
10   electrical connection to the functional element hermetically sealed within the cavity, and depicts the completed MEMS package produced by the method of FIGS. 1-9.

FIGS. 4A-9A depict an embodiment similar to FIGS. 4-9, but including the formation of an oxide layer on a surface of the silicon portion and within the recessed cavity before the metal connectors are formed, and FIG. 9A further depicts the  
15   resulting completed MEMS package.

FIGS. 10 and 10A depict embodiments of the present invention including a passivation layer.

FIGS. 11 and 11A depict embodiments of the present invention including a single wire bond pad connecting a hermetically sealed functional element to a metal  
20   lead in another cavity.

FIG. 12 is a flow chart for methods of the present invention.

### **Detailed Description**

The method of the present invention uses an SOI wafer as wafer-level packaging material, and puts electrical feed-throughs through the SOI wafer. The  
25   processing is simple, no high temperature steps are required, and the resulting die is

small and thin, and does not require complex packaging to achieve cavity hermeticity.

The method will be described with reference to FIGS. 1-9, which schematically depict the method by which a MEMS device is packaged according to the present invention.

As depicted in FIG. 1, a first substrate 10 is provided. This wafer or substrate 10 may

5 be any silicon or non-silicon wafer, such as a Pyrex glass wafer. As depicted in FIG. 2,

the functional element 12 is formed on the surface 11 of the first substrate 10. The term

“functional element” refers to the microelectromechanical device, which may for

example be a circuit, sensor or actuator. The method for forming the functional element

12 on the first substrate 10 may be by any method known to one skilled in the art. Once

10 formed, the functional element 12 will have a thickness  $t_1$ . At least two metal leads 14

are formed on the surface 11 of the first substrate 10, at least one of those metal leads 14

being connected to the functional element 12. In one embodiment of the present

invention, shown in FIG. 2, two metal leads 14 are formed and connected to the

functional element 12. It should be understood by those skilled in the art that a typical

15 semiconductor device includes a plurality of functional elements 12, each having

electrical connections in and out of the functional element 12. The metal leads 14

generally comprise a soft metal, for example aluminum, gold, aluminum alloys, or gold

alloys. When formed, the metal leads 14 have a thickness  $t_2$ .

As depicted in FIG. 3, a second substrate 20 is provided, which is a SOI

20 wafer. SOI wafer refers to a silicon-on-insulator in which a thin oxide layer 22 is buried

within the silicon substrate 24. To state another way, SOI substrate 20 comprises a first

silicon portion 24a, a second silicon portion 24b, and a silicon oxide layer 22

therebetween. SOI wafers are well known in the art of semiconductor devices.

As depicted in FIG. 4, a recessed cavity 26 is formed in the first silicon

25 portion 24a of the second SOI substrate 20. Any known method for material removal

may be used in the method of the present invention to form the recessed cavity 26. For example, the recessed cavity 26 may be formed by reactive ion etching (RIE), which may use for example a dry plasma of  $\text{SF}_6$ . By way of further example, wet chemical etching may be used, for example using KOH. The recessed cavity 26 is etched to a  
5 depth  $d$  greater than the thickness  $t_1$  of the functional element 12 formed on the first substrate 10. In another embodiment of the present invention, depicted in FIG. 4A, an oxide layer 28 is grown on the non-recessed surface 25 of the first silicon portion 24a and within the recessed cavity 26. This oxide layer 28 may be grown by any method known to those skilled in the art, such as by thermal oxidation. The oxide layer 28  
10 provides electrical isolation between the electrical connectors. In remaining FIGS. 5-9, the device is shown without the oxide layer 28, and in FIGS. 5A-9A, the device is shown with the oxide layer 28.

As shown in FIGS. 5 and 5A, metal connectors 30 are formed in the recessed cavity 26. The metal connectors 30 are each positioned to correspond to a  
15 respective metal lead 14 formed on the first substrate 10. As with the metal leads 14, the metal connectors 30 may comprise a soft metal, such as aluminum, gold or an alloy of aluminum or gold. Advantageously, the metal connectors 30 comprise the same metal as the metal leads 14. When formed, the metal connectors 30 have a thickness  $t_3$ . Referring back to FIGS. 4 and 4A, the depth  $d$  of the recessed cavity 26 should be less  
20 than the combined thickness  $t_2 + t_3$  of the metal leads 14 and metal connectors 30. The metal connectors 30 may be formed by any method known to those skilled in the art of semiconductor device fabrication.

FIG. 6 depicts the bonding of the second SOI substrate 20 to the first substrate 10. The non-recessed surface 25 of the SOI substrate 20 is bonded to the  
25 surface 11 of the first substrate 10. The metal leads 14 on the first substrate 10 are

generally or partially aligned with the metal connectors 30 formed within the recessed cavity 26 of the second SOI substrate 20. Because the depth  $d$  of the recessed cavity 26 is less than the combined thicknesses  $t_2$  and  $t_3$  of the metal leads 14 and metal connectors 30, a metal lead 14 and respective metal connector 30 are fused together such that the resulting combined thickness is equal to the depth  $d$  of the recessed cavity 26. By virtue of the bonding of the non-recessed surface 25 of the second SOI substrate 20 to the first substrate 10, the recessed cavity 26 is hermetically sealed from the environment. A space 32 remains within the sealed recessed cavity 26 above the functional element 12 by virtue of the depth  $d$  of the recessed cavity 26 being greater than the thickness  $t_1$  of the functional element 12. The functional element 12 is thus enclosed in the hermetically sealed cavity 26 and movable therein. In the embodiment depicted in FIG. 6A, the oxide layer 28 formed on the non-recessed surface 25 of the second SOI substrate 20 is bonded to the first substrate 10. The same effect of a hermetically sealed cavity 26 is achieved in this embodiment.

In exemplary embodiments of the present invention, the bonding of the substrates 10, 20 may be by room temperature fusion bonding or anodic bonding. In room temperature fusion bonding, which is advantageously used when the first substrate 10 is a silicon-base substrate, the wafers 10, 20 are cleaned and then bonded together by applying a pressure in the range of about 800-1400 pounds. The bonded wafers are then cured at room temperature, for example, for a period of a few days. If it is desirable to accelerate the curing of the wafer bond, a low temperature annealing may be utilized, wherein the temperature is less than a temperature that would negatively effect the metal portions of the device, for example around 200°C. Alternatively, the bonding may be anodic bonding, which may be advantageously used where the first substrate 10 is a Pyrex glass or other glass substrate. Anodic bonding generally comprises applying an



electrical bias in the range of about 100-1000 V, for example about 800 V to the wafers 10, 20 in contact while applying a temperature in the range of about 300-500°C.

As shown in FIGS. 7 and 7A, the second silicon portion 24b of the second SOI substrate 20 not bonded to the first substrate 10 is removed to expose the  
5 buried oxide layer 22. The silicon may be removed by any method known to those skilled in the art, such as the RIE and wet etch methods discussed above with respect to formation of the recessed cavity 26.

As shown in FIGS. 8 and 8A, vias 34 are formed through the second SOI substrate 20 to expose the metal connectors 30 within the recessed cavity 26. The  
10 formation of the vias 34 will allow for electrical connections to be made through the SOI substrate 20 to the metal connectors 30 and metal leads 14, and thus to the functional element 12 sealed within the cavity 26, but does not break the hermetic seal and expose the functional element 12 to the environment. The vias 34 may be etched by any method known to those skilled in the art. For example, the etching of the vias 34  
15 may include a two-step process in which one method is used to etch through the oxide layer 22 of the SOI substrate 20, and a second method is used to etch through the silicon portion 24a of the SOI substrate 20. By way of further example, an HF-containing solution may be used to etch the oxide layer 22, and the wet chemical etching or RIE methods discussed above may be used to etch through the Si layer 24a.

FIGS. 9 and 9A depict the patterning of metal pads 36 for forming  
20 electrical connections with the functional element 12. The wire bond pads 36 are formed within the vias 34 on the metal connectors 30 and extend over a portion of the oxide layer 22 of the second SOI substrate 20. The formation of the metal pads 36 may be by any method known to those skilled in the art, and generally includes CVD and  
25 PVD methods. By way of further example, the metal pads 36 may be aluminum with a

barrier/adhesion liner or may be gold with an adhesion liner. For example, the metal pads may be Al/Ti/TiN or Au/Cr.

There is thus formed a complete MEMS package 40 in which electrical connections are made by the metal pads 36, through the metal connectors 30, through the metal leads 14 to the functional element 12, and vice versa. No complex processing nor high temperatures were required in the above-described process. Moreover, the functional element 12 is electrically connected while being hermetically sealed within the package 40.

Another embodiment of a method and resulting MEMS package 40' of the present invention is depicted in FIGS. 10 and 10A. The MEMS package 40' may include a passivation layer 42 formed over a portion of the wire bond metal pads 36 and over the exposed oxide portion 22 of the second SOI substrate 20. In this embodiment, vias 44 are formed above at least a portion of the wire bond metal pads 36. The passivation layer 42 provides additional contamination control for the device 40'. By way of example, the final passivation layer 42 is a plasma nitride, and may be formed by blanket PECVD using silane and ammonia. The via or pad openings 44 over the metal pads 36 may be formed by any material removal process known to those skilled in the art.

FIGS. 11 and 11A depict yet another embodiment of a method and resulting MEMS package 40" of the present invention. In this embodiment, the functional element 12 and one metal lead 14a and metal connector 30a are enclosed within one recessed cavity 26a, and a second recessed cavity 26b is formed in the second SOI substrate 20 for a second metal lead 14b and metal connector 30b. Vias 34 are formed through oxide layer 22 and silicon portion 24a to each of the metal connectors 30a, 30b. A wire bond pad 36 is formed in the vias 34 in the active SOI

substrate 20 and over oxide layer 22 thereby using the top 23 of the oxide 22 as a temporary passage for the metal line.

FIG. 12 provides a flow chart for an exemplary embodiment of the method of the present invention. To form the non-active substrate, the first step is to provide the first substrate. The next step is to form the functional element or elements and the metal leads on the first substrate. To form the active substrate, the first step is to provide a second SOI substrate having a first silicon layer, a second silicon layer, and a buried oxide layer therebetween. The second step is to then etch a recess in the first silicon layer to form the recessed cavity. The third step is to pattern the metal connectors within that recessed cavity. An optional fourth step may include growing an oxide layer on the first silicon layer and within the recessed cavity. Having formed the first substrate with a functional element and metal leads thereon, and having formed a second SOI substrate having at least one recessed cavity in a silicon portion thereof with metal connectors therein, the two substrates may then be bonded together by generally matching the position of the metal leads to the position of the metal connectors and bonding them together as well as bonding the non-recessed surface of the first silicon layer to the first substrate. Next, the second silicon layer of the SOI substrate is then removed to expose the buried oxide layer. Vias are then etched through the oxide layer and the first silicon layer to expose the metal connectors. Metal pads are then patterned within the vias and at least partially over the oxide layer. Optionally, a final passivation layer may be formed over the metal pads and oxide layer to provide additional contamination resistance. There is thus provided a packaging method for MEMS that allows for a small footprint, small chip outline, low temperature processing, hermetic sealing of the functional element and at a low cost compared to prior techniques.

While the present invention has been illustrated by the description of an embodiment thereof, and while the embodiment has been described in considerable detail, it is not intended to restrict or in any way limit the scope of the appended claims to such detail. Additional advantages and modifications will readily appear to those skilled in the art. The invention in its broader aspects is therefore not limited to the specific details, representative apparatus and method and illustrative examples shown and described. Accordingly, departures may be made from such details without departing from the scope or spirit of applicant's general inventive concept.

WHAT IS CLAIMED IS: